The Effect of High Temperature Annealing on Fluorine Distribution Profile and Electro-Physical Properties of Thin Gate Oxide Fluorinated by Silicon Dioxide RIE in CF₄ Plasma

Małgorzata Kalisz, Grzegorz Głuszko, and Romuald B. Beck

Abstract—This study describes the effects of high temperature annealing performed on structures fluorinated during initial silicon dioxide reactive ion etching (RIE) process in CF₄ plasma prior to the plasma enhanced chemical vapour deposition (PECVD) of the final oxide. The obtained results show that fluorine incorporated at the PECVD oxide/Si interface during RIE is very stable even at high temperatures. Application of fluorination and high temperature annealing during oxide layer fabrication significantly improved the properties of the interface (Dit mb decreased), as well as those of the bulk of the oxide layer (Qeff decreased). The integrity of the oxide (higher Vbd) and its uniformity (Vbd distribution) are also improved.

Keywords—capacitance-voltage characteristics, current-voltage characteristics, fluorine plasma, high temperature annealing process, radio frequency reactive ion etching.

1. Introduction

A key issue of ultra-large-scale-integration technology (ULSI) is the quality of thin silicon dioxide layer used in the devices. Today, oxide thickness less than 80 Å and oxidation temperatures at about 800–900°C are required as the semiconductor industry pushes toward 1 Gbit memory chips and beyond. However, good electrical properties generally require high temperature conditions either during oxidation or as postoxidation annealing (POA) [1]. At low temperatures, ultrathin SiO₂ films prepared by the conventional plasma enhanced vapour deposition (PEVD) process do not represent satisfactory properties, e.g., they are characterized by high leakage currents and high fixed charge density. It has been demonstrated, e.g., in [1]–[6] that incorporation of small amounts of fluorine into SiO₂ can be an efficient way to improve the electrical parameters of SiO₂/Si interface.

Several ways of fluorine introduction into gate oxide, including among others: in-situ NF₃ oxidation [4] and ion implantation [5], have been tried so far. Another useful technique to improve the quality of low temperature SiO₂ is high thermal annealing process.

It, thus, seems tempting to apply both of these techniques in order to get the best results possible. The problem with such an approach is that high temperature annealing of fluorinated oxides fabricated by means of the above mentioned processes seriously affects the F concentration in the oxides – as fluorine atoms escape from fluorinated gate oxides during high temperature annealing [7].

In our previous work, it has been reported that fluorination by means of reactive ion etching (RIE) in CF₄ plasma is an efficient method of manufacturing quite good quality oxides [8].

In this work, we study the effects of high temperature annealing on structures fluorinated during initial silicon dioxide reactive ion etching in CF₄ plasma prior to the plasma enhanced chemical vapour deposition (PECVD) of the final oxide.

2. Experiments

The p-type, boron-doped (100)-oriented silicon wafers with the resistivity of 4–10 Ωcm were cleaned using standard procedures prior to oxidation.

The PECVD and RIE processes were performed in conventional RF Oxford PlasmaLab systems. The 13 nm thick initial oxide was deposited by means of PECVD at 300°C for 30 s with RF power equal to 10 W. The obtained SiO₂ film was then reactively etched for 2 min in a RIE tool at room temperature in CF₄ (50 ml/min) plasma generated with 160 W RF signal. Afterwards, the final oxide layer was deposited during PECVD at 300°C. Then, in split experiment, some of the samples were annealed in Ar at 1100°C for 30 min. The complete matrix of experiments is shown in Table 1.

For all samples, except of the control one, the fluorine distribution profiles and their concentration in the dielectric layer have been measured by ultra low energy-secondary ion mass spectroscopy (ULE-SIMS).

In order to use electrical characterization methods for evaluation of electro-physical properties, metal-oxide-semiconductor (MOS) test structures were fabricated with
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Table 1
Parameters of all processes used during experiments

<table>
<thead>
<tr>
<th>Type of sample</th>
<th>Reactive ion etching (RIE) in RF CF$_4$ plasma</th>
<th>Final SiO$_2$ deposition in PECVD</th>
<th>Thermal annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>50</td>
<td>200</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>50</td>
<td>200</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>–</td>
<td>–</td>
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</tr>
</tbody>
</table>

3. Results and Discussion

3.1. SIMS Characterization of Fluorine Content

It has already been established before (e.g., in [9]) that reactive ion etching in fluorine plasma can be effectively used for fabricating layers containing high concentrations of fluorine atoms. Direct application of high temperature to such a layer causes fluorine atoms to escape from the fluorinated film. Thin film of silicon oxide deposited at low temperature (300°C) on top of the fluorine-rich layer prevents them from escaping from the fluorinated layer during the subsequent high temperature annealing process.

![Fig. 1](image)

Fig. 1. The comparison of fluorine distribution profiles before and after high temperature annealing.

As presented in Fig. 1, the high temperature annealing performed in Ar at 1100°C, for 30 min had almost no effect on fluorine profile in the studied structures. The only change observed is marginal sharpening of the fluorine profile. This indicates that fluorine remains stable during high temperature annealing at its original location at the PECVD SiO$_2$/Si interface.

3.2. Electrical Characterization

The effect of fluorine incorporation into deposited silicon dioxide and of high temperature annealing was easily noticeable on both types of the electrical characteristics studied, i.e., capacitance-voltage ($C-V$) and current-voltage ($I-V$) characteristics of test metal-oxide-semiconductor capacitors.

3.2.1. Analysis of $C-V$ Characteristics

As expected, the very high temperature annealing causes improvement of the $C-V$ curves in both of the studied cases (Fig. 2). This improvement seems to be more spectacular for non-fluorinated sample in which apart from the decrease of the voltage shift (expressed, e.g., in terms $V_{fb} = 0$) also the frequency dispersion in the inversion region has been significantly reduced.

One may, however, notice also some consequences of high temperature annealing on the fluorinated samples. The beneficial effects of high temperature annealing for attaining more robust oxides have been attributed to its possible ability to remove defects and damages existing in the bulk of the PECVD silicon dioxide layer. Application of high temperature annealing causes a reduction of both, $D_{it mb}$ and $Q_{eff}$ (see Table 2 and Fig. 3).

Similarly to the results presented in [8], within the course of this work it has been established that the fluorine atoms incorporated into the interface of SiO$_2$/Si improve the electrical parameters of silicon dioxide layer. However, the result of the high temperature annealing is still clearly noticeable on the measured $C-V$ curves as well as in the values of the evaluated electrical parameters, i.e., $D_{it mb}$ and $Q_{eff}$. This means that the latter process is still capable of removing some defects existing in the bulk of PECVD silicon dioxide layer.

It has to be realized, however, that the degree of improvement due to high temperature annealing is by far smaller than that due to fluorination of the silicon substrate surface.

It is also worth mentioning that the degree of $Q_{eff}$ changes is much higher than that of $D_{it mb}$, which means that fluorine presence in the structure is especially beneficial for curing
The Effect of High Temperature Annealing on Fluorine Distribution Profile and Electro-Physical Properties of Thin Gate Oxide Fluorinated... 

Fig. 2. The $C-V$ characteristics of samples fabricated in different ways: (a) control sample, (b) control sample annealed, (c) RIE fluorinated but not annealed, and (d) RIE fluorinated and annealed.

Fig. 3. Dependence of $Q_{\text{eff}}$ and $D_{\text{itmb}}$ on the method of fabrication the MOS test structure.

Table 2

<table>
<thead>
<tr>
<th>Sample type</th>
<th>Control</th>
<th>Control annealed</th>
<th>RIE fluorinated</th>
<th>RIE fluorinated and annealed</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C-V$ curves analysis at $E_{\text{ox}} = 3.9$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$N_A$ [cm$^{-3}$]</td>
<td>1.73·10$^{15}$</td>
<td>1.17·10$^{15}$</td>
<td>0.43·10$^{15}$</td>
<td>1.4·10$^{15}$</td>
</tr>
<tr>
<td>$V_{fb}$ [V]</td>
<td>-4.15</td>
<td>-3.28</td>
<td>-1.42</td>
<td>-1.30</td>
</tr>
<tr>
<td>$V_{mb}$ [V]</td>
<td>-3.4</td>
<td>-2.7</td>
<td>-0.95</td>
<td>-0.86</td>
</tr>
<tr>
<td>$Q_{\text{eff}}/q$ [cm$^{-2}$]</td>
<td>35.8·10$^{11}$</td>
<td>28.4·10$^{11}$</td>
<td>7.7·10$^{11}$</td>
<td>7.0·10$^{11}$</td>
</tr>
<tr>
<td>$D_{\text{itmb}}$ [1/eV cm$^2$]</td>
<td>10.3·10$^{11}$</td>
<td>8.17·10$^{11}$</td>
<td>5.7·10$^{11}$</td>
<td>5.18·10$^{11}$</td>
</tr>
</tbody>
</table>

the defects within the volume of the gate oxide, while high temperature annealing seems to be similarly effective in both areas (interface and volume of the oxide).

3.2.2. Analysis of $I-V$ Characteristics

As shown in Fig. 4, application of high temperature annealing in control samples improves a little the statistics of breakdown events at the expense of higher leakage current, while having almost no effect on $V_{bd}$ values.

Introduction of fluorine to the PECVD oxide improves both, $V_{bd}$ values and their distribution. When high temperature annealing is additionally performed on fluorinated structures, we obtain even more narrow $V_{bd}$ distribution, as well as higher $V_{bd}$ values. Practically, no changes in the leakage currents values are observed.

Hence, also from the perspective of the electro-physical properties that are manifested on $I-V$ characteristics, simultaneous application of both, fluorination and high temperature annealing is advantageous in comparison to the application of any of these methods individually.
4. Conclusions

The results obtained during this study show that fluorine incorporated at the PECVD oxide/Si interface by means of RIE is very stable even at high temperatures. This effect allows combining the fluorination and high temperature annealing in order to improve the electro-physical properties of the low temperature oxide (e.g., PECVD oxide). We have also demonstrated that there are several advantages of the application of such combination. The properties of the SiO$_2$/Si interface ($D_{amb}$ decreased) and the bulk of the oxide layer ($Q_{eff}$ decreased) are significantly improved. The integrity of the oxide (higher $V_{bd}$) and its uniformity ($V_{bd}$ distribution) are also improved.

The improvement of the electro-physical properties of the SiO$_2$-Si systems obtained due to application of both studied steps (fluorination and high temperature annealing) is in all studied cases better than using one of these steps only.

References


Małgorzata Kalisz – for biography, see this issue, p. 23.

Grzegorz Głuszko and Romuald B. Beck – for biographies, see this issue, p. 24.